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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,096	06/22/2001	Lauren B. Wenzl	X-662 US	7929

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EXAMINER	
ZHEN, LI B	
ART UNIT	**PAPER NUMBER**
2126	3

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,096	WENZL, LAUREN B.	
	Examiner	Art Unit	
	Li B. Zhen	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 11 are pending in the application.

Drawings

2. Drawings filed on June 22, 2001 are approved by the Draftsperson under 37 CFR 1.84 or 1.152.

Claim Rejections - 35 USC § 101

3. Claims 8 – 11 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

4. Claims 8 – 11 are directed to method steps which can be practiced mentally in conjunction with pen and paper, therefore they are directed to non-statutory subject matter. Specifically, as claimed, it is uncertain what performs each of the claimed method steps. Moreover, each of the claimed steps, inter alia, identifying, storing, determining and configuring, can be practiced mentally in conjunctions with pen and paper. The claimed steps do not define a machine or computer implemented process [see MPEP 2106]. Therefore, the claimed invention is directed to non-statutory subject matter. (The examiner suggests applicant to change "method" to "computer implemented methods" in the preamble to overcome the outstanding 35 U.S.C. 101 rejection).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1 – 7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent NO. 6,721,872 to Dunlop.**

7. As to claim 1, Dunlop teaches an interface [reconfigurable network interface architecture 10, Fig. 1; col. 3, lines 12 – 35] for an electronic device [host device 18, Fig. 1; col. 3, lines 12 – 50] being coupled to an external device [network 16, Fig. 1, col. 3, lines 12 – 50; host device can communicate with other devices over the selected network; col. 2, lines 20 – 45], the interface including:

a configurable hardware interface [architecture 10 combines a programmable hardware (HW) device; col. 3, lines 12 – 50], wherein the configurable hardware interface includes:

a programmable logic device (PLD) [a programmable logic device (PLD) such as a field programmable gate array (FPGA) 12, Fig. 1; col. 3, lines 12 – 36];

a memory coupled to the PLD [FPGA 12 has an associated configuration memory 24; col. 3, lines 60 – 67];

a control interface for controlling the PLD and the memory [a programmable software (SW) device in the form of a processor 14; col. 3, lines 13 – 60]; and

a communication interface [communication subsystem 22 operatively connects the FPGA 12 and the processor 14 to one another, and with the host device 18 and the physical medium of the network 16, Fig. 2; col. 3, lines 50 – 60] for receiving information from the external device and enabling the control interface [In response to information identifying a selected network, the processor is arranged to load corresponding network protocol data from the configuration memory and the processor memory into the logic device and the processor, so that the host device can communicate with other devices over the selected network; col. 2, lines 20 – 47]; and

a storage component [configuration memory] for storing a bitstream that configures the configurable hardware interface to implement a driver of the external device [configuration memory 24 is arranged to store certain data associated with protocols of networks to which a connection port 12a of the FPGA 12 is adapted to be coupled. Such data may pertain to signaling format and size of data frames to be transmitted and received by the host device 18 over the network 16, error checking algorithms to be performed on data carried by the network, and other digital logic processes to be performed on the network data; col. 3, line 60 – col. 4, line 16].

8. As to claim 2, Dunlop teaches the storage component includes volatile memory [random access memory (RAM) 32 associated with the processor 14, Fig. 3; col. 4, lines 42 – 56].

9. As to claim 3, Dunlop teaches the storage component includes static random access memory [configuration memory 24 and the program memory 33 are in the form of "flash" or other kind of non-volatile memories; col. 7, lines 12 – 30].

10. As to claim 4, Dunlop teaches the communication interface includes one of a universal serial bus, a parallel port connector, a serial port connector [conversion to a 4-bit serial interface when transmitting into the network 16; col. 7, lines 55 – 65], and a small computer system interface (SCSI).

11. As to claim 5, Dunlop teaches the communication interface establishes synchronous communication between the electronic device and the external device [data communication path is coupled to the processor and to the logic device, and the communication path is arranged to be coupled to a host device for transferring data between the host device and a network to which the logic device is coupled; col. 2, lines 20 – 46].

12. As to claim 6, Dunlop teaches the memory includes at least one lookup table [Module 26 sets the FPGA 12 into a configured state by generating addresses (path 3)

for the configuration memory 24 corresponding to the identified set of stored protocol data; col. 6, lines 38 – 57].

13. As to claim 7, Dunlop teaches including at least one of an Ethernet interface [prototype card was configured to support two protocols, namely, (1) Ethernet at 10/100 Mbps, and (2) DSL running at 1.5 Mbps on receive, and at 512 Kbps on transmit; col. 7, lines 43 – 55], a modem interface, and a custom interface for communicating with the external device.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. **Claims 8 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunlop in view of U.S. Patent Application Publication NO. 2002/0095501 to Chiloyan.**

16. As to claim 8, Dunlop teaches the invention substantially as claimed including a method of facilitating communication between two devices [network 16, Fig. 1, col. 3, lines 12 – 50; host device can communicate with other devices over the selected network; col. 2, lines 20 – 45], the method comprising:

identifying a host device [host device 18, Fig. 1; col. 3, lines 12 – 50], from the two devices, that controls communication between the two devices [a programmable software (SW) device in the form of a processor 14; col. 3, lines 13 – 60];

identifying a peripheral device that accepts commands from the host device [identifying a desired network protocol implementation for the NIC 20, by signaling the configuration memory 24 and the program memory 33 to load corresponding program data into the FPGA 12 and the processor 14; col. 4, lines 1 – 15];

storing a plurality of bitstreams in the host device, the plurality of bitstreams corresponding to predetermined drivers [configuration memory 24 is arranged to store certain data associated with protocols of networks to which a connection port 12a of the FPGA 12 is adapted to be coupled. Such data may pertain to signaling format and size of data frames to be transmitted and received by the host device 18 over the network 16, error checking algorithms to be performed on data carried by the network, and other digital logic processes to be performed on the network data; col. 3, line 60 – col. 4, line 16]; and

configuring a programmable logic device (PLD) [a programmable logic device (PLD) such as a field programmable gate array (FPGA) 12, Fig. 1; col. 3, lines 12 – 36] in the host device with the bitstream to implement the driver of the peripheral device [In response to information identifying a selected network, the processor is arranged to load corresponding network protocol data from the configuration memory and the processor memory into the logic device and the processor, so that the host device can communicate with other devices over the selected network; col. 2, lines 20 – 47].

17. Although Dunlop teaches the invention substantially as claimed, Dunlop does not teaches determining whether one of the predetermined drivers is a driver of the peripheral device, selecting that bitstream corresponding to the driver of the peripherals device if one of the predetermined drivers is the driver of the peripheral device, otherwise, directing the host device to receive a bitstream from the peripheral device.

However, Chiloyan teaches determining whether one of the predetermined drivers is a driver of the peripheral device [at a decision step 64, if the peripheral was previously installed, Fig. 2; paragraph (0044), p. 5], selecting that bitstream corresponding to the driver of the peripherals device if one of the predetermined drivers is the driver of the peripheral device [If the peripheral device was previously installed on personal computer 20...then operating system 35 simply loads the device driver and/or other software into memory; paragraph (0044), p. 5], otherwise, directing the host device to receive a bitstream from the peripheral device [If the peripheral device has not been registered on personal computer 20, or if the device driver and/or other software is no longer available on personal computer 20, then operating system 35 performs a decision step 66 to determine whether a network address is stored in the peripheral device; paragraph (0045), p. 5]

18. It would have been obvious to a person of ordinarily skilled in the art at the time of the invention to apply the teaching determining if one of the predetermined drivers is a driver of the peripheral device, selecting that driver if it is, otherwise, receive a driver from the peripheral device as taught by Chiloyan to the invention of Dunlop because this eliminates the need for the user to insert a CD-ROM or floppy disk into a host

computing device, or otherwise manually obtain the required software and provides an improved plug-and-play capability [paragraph (0009), p. 2 of Chiloyan].

19. As to claim 9, Dunlop as modified teaches storing a plurality of designations in the PLD [configuration memory 24 is arranged to store certain data associated with protocols of networks to which a connection port 12a of the FPGA 12 is adapted to be coupled. Such data may pertain to signaling format and size of data frames to be transmitted and received by the host device 18 over the network 16, error checking algorithms to be performed on data carried by the network, and other digital logic processes to be performed on the network data; col. 3, line 60 – col. 4, line 16 of Dunlop], wherein each designation corresponds to one of the plurality of bitstreams, wherein determining includes searching the plurality of designations [operating system checks whether the peripheral information is listed in the operating system's device registry; paragraph (0044), p. 5 of Chiloyan].

20. As to claim 10, this is rejected for the same reasons as claim 6 above.

21. As to 11, Dunlop as modified teaches each designation includes an addresses for one of the plurality of bitstreams stored in the host device [operating system 35 performs a decision step 66 to determine whether a network address is stored in the peripheral device; paragraph (0045) – (0046), p. 5 of Chiloyan], and wherein selecting includes accessing an address in the host device for the bitstream to implement the

driver of the peripheral device [if a network address is stored in the peripheral device, then operating system 35 performs a step 70 to initiate download of the device driver and/or other software from a remote device accessed via the network address; paragraph (0045) - (0046), p. 5 of Chiloyan].

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent NO. 6,480,027 to Ngai teaches driver circuitry for programmable logic devices.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (703) 305-3406. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Li B. Zhen
Examiner
Art Unit 2126

lbz
April 16, 2004

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